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MS-7786 Ver:1.0

CPU:

AMD FM1

System Chipset:

AMD - Hudson D2

On Board Chipset:

USB2.0 RearX4 FrontX6

SATAII X6

LPC Super I/O --F71868AD

LAN-Realtek 8105E Co-lay8111E

Azalia CODEC - Realtek ALC887 Co-lay VT1708S

Main Memory:

DDR III *2 (Max 16G)

Expansion Slots:

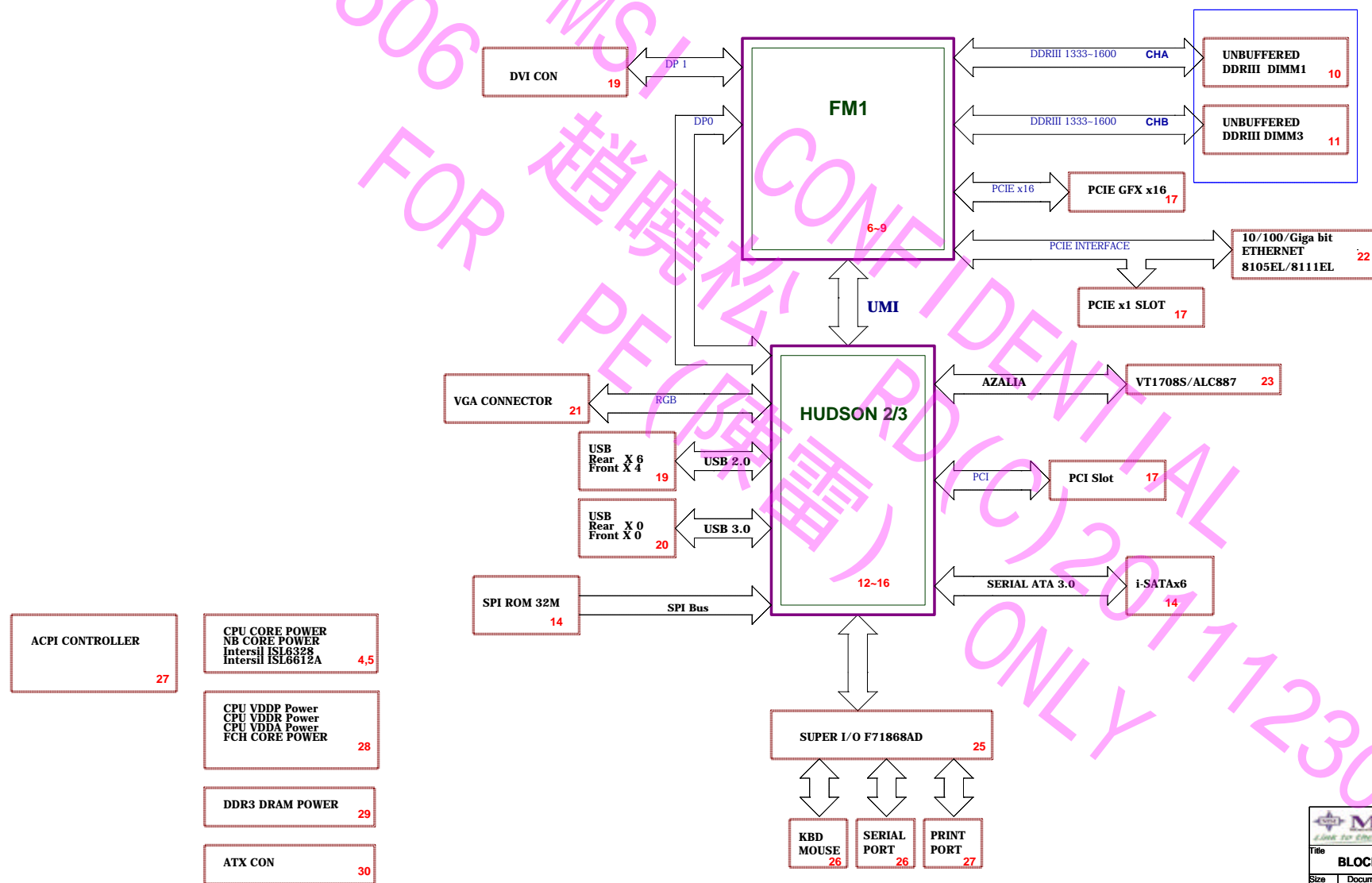
PCI Express X16 Slot * 1

PCI Express X1 Slot * 1

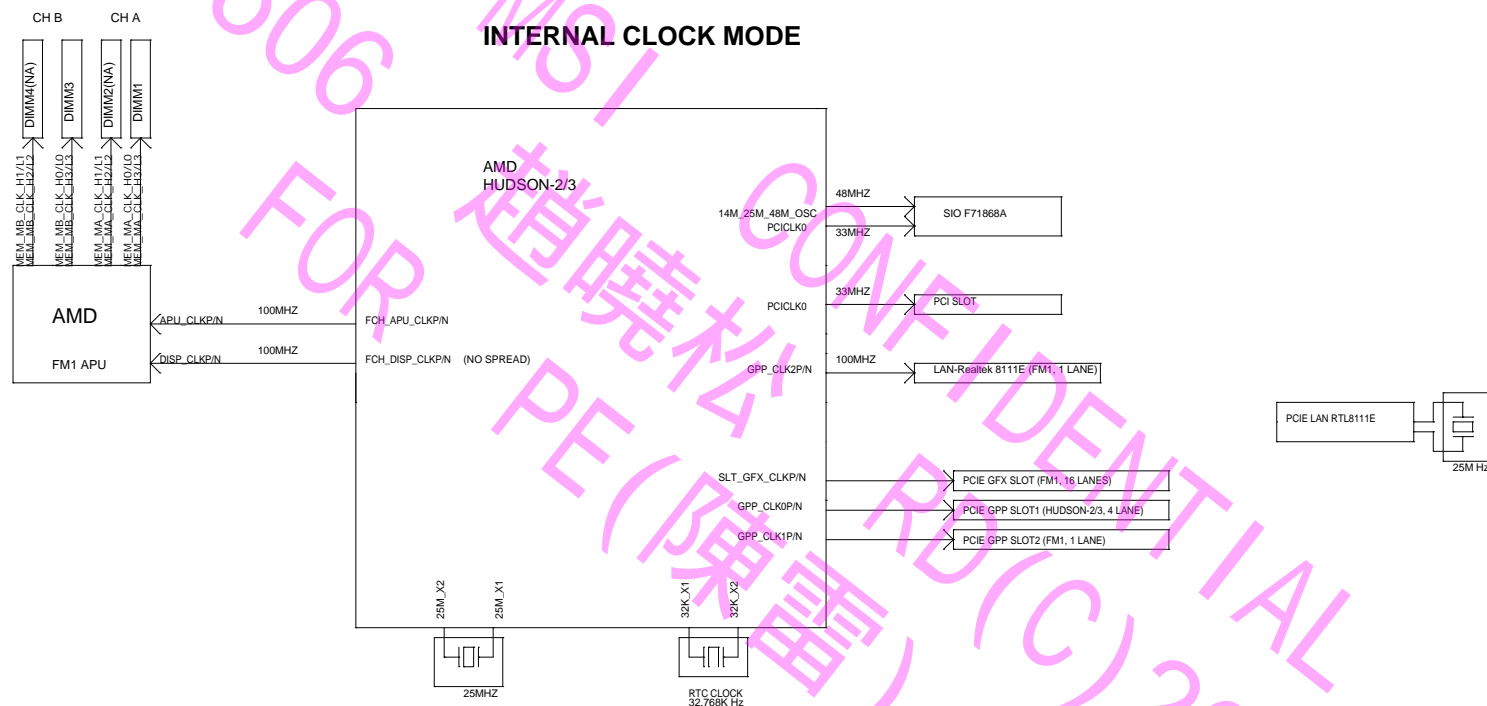
VRM

Controller - Intersil ISL6328 3+1 Phase

FUSION BLOCK DIAGRAM

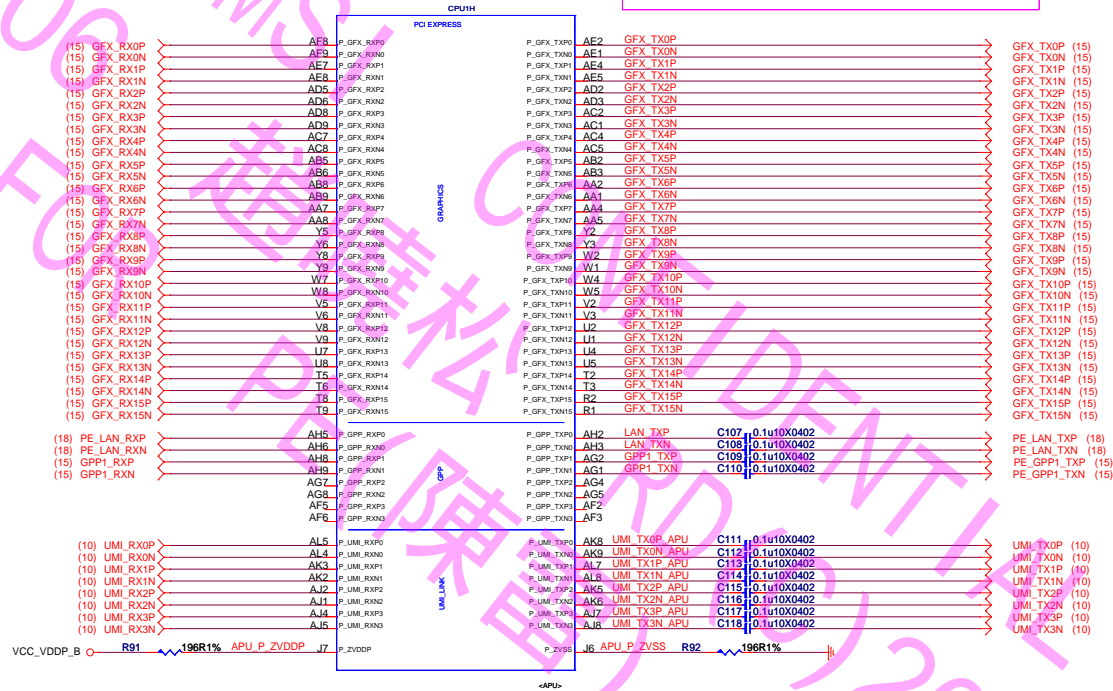


00015506 MS1
FOR 趙曉松 (陳雷)
CONFIDENTIAL
ONLY
20111230007



FM1 PCIE I/F

mach@CRB PCIE AC Capacitors:75nF to 200nF
Layout: PLACE CAPS WITH APU < 1 INCH
ROUTE ALL PCIE AS 85OHM +/-10%



FM1DDR3 V/F

(8) MEM_MA_DQS_L[7..0]

(8) MEM_MA_DQS_H[7..0]

(8) MEM_MA_DM[7..0]

(8) MEM_MA_ADD[15..0]

(8) MEM_MA_BANK0
(8) MEM_MA_BANK1
(8) MEM_MA_BANK2

MEM_MA_DM0
MEM_MA_DM1
MEM_MA_DM2
MEM_MA_DM3
MEM_MA_DM4
MEM_MA_DM5
MEM_MA_DM6
MEM_MA_DM7

MEM_MA_DQS_H0
MEM_MA_DQS_L0
MEM_MA_DQS_H1
MEM_MA_DQS_L1
MEM_MA_DQS_H2
MEM_MA_DQS_L2
MEM_MA_DQS_H3
MEM_MA_DQS_L3
MEM_MA_DQS_H4
MEM_MA_DQS_L4
MEM_MA_DQS_H5
MEM_MA_DQS_L5
MEM_MA_DQS_H6
MEM_MA_DQS_L6
MEM_MA_DQS_H7
MEM_MA_DQS_L7

machCLOCK assignment can be changed

(8) MEM_MA_CLK_H0
(8) MEM_MA_CLK_L0

(8) MEM_MA_CLK_H0
(8) MEM_MA_CLK_L0

(8) MEM_MA_CLK_H3
(8) MEM_MA_CLK_L3

(8) MEM_MA_CLK_H3
(8) MEM_MA_CLK_L3

(8) MEM_MA_CKE0
(8) MEM_MA_CKE1

(8) MEM_MA_CKE0
(8) MEM_MA_CKE1

(8) MEM_MA1_ODT0
(8) MEM_MA1_ODT1

(8) MEM_MA1_ODT0
(8) MEM_MA1_ODT1

(8) MEM_MA1_CS_L0
(8) MEM_MA1_CS_L1

(8) MEM_MA1_CS_L0
(8) MEM_MA1_CS_L1

(8) MEM_MA_RAS_L
(8) MEM_MA_CAS_L

(8) MEM_MA_RAS_L
(8) MEM_MA_CAS_L

(8) MEM_MA_RESET#
(8) MEM_MA_HOT#

(8) MEM_MA_RESET#
(8) MEM_MA_HOT#

APU_M_VREF

VCC_DDR

machu603777trace width???

Layout:
Place within 1.5" of APU

7

4

3

2

1

CPU1A

MEMORY CHANNEL A

MA_ADD0

MA_ADD1

MA_ADD2

MA_ADD3

MA_ADD4

MA_ADD5

MA_ADD6

MA_ADD7

MA_ADD8

MA_ADD9

MA_ADD10

MA_ADD11

MA_ADD12

MA_ADD13

MA_ADD14

MA_ADD15

MA_BANK0

MA_BANK1

MA_BANK2

MA_DM0

MA_DM1

MA_DM2

MA_DM3

MA_DM4

MA_DM5

MA_DM6

MA_DM7

MA_DQS_H0

MA_DQS_L0

MA_DQS_H1

MA_DQS_L1

MA_DQS_H2

MA_DQS_L2

MA_DQS_H3

MA_DQS_L3

MA_DQS_H4

MA_DQS_L4

MA_DQS_H5

MA_DQS_L5

MA_DQS_H6

MA_DQS_L6

MA_DQS_H7

MA_DQS_L7

MA_CLK_H0

MA_CLK_L0

MA_CLK_H1

MA_CLK_L1

MA_CLK_H2

MA_CLK_L2

MA_CLK_H3

MA_CLK_L3

MA_CKE0

MA_CKE1

MA1_ODT0

MA1_ODT1

MA1_CS_L0

MA1_CS_L1

MA_RAS_L

MA_CAS_L

MA_WE_L

MA_RESET#

MA_HOT#

MA_VREF

MA_VDDIO

MA_VDDIO

MA_VDDIO

MA_DATA0

MA_DATA1

MA_DATA2

MA_DATA3

MA_DATA4

MA_DATA5

MA_DATA6

MA_DATA7

MA_DATA8

MA_DATA9

MA_DATA10

MA_DATA11

MA_DATA12

MA_DATA13

MA_DATA14

MA_DATA15

MA_DATA16

MA_DATA17

MA_DATA18

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MA_DATA161

MA_DATA162

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MA_DATA165

MA_DATA166

MA_DATA167

MA_DATA168

MA_DATA169

MA_DATA170

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MA_DATA175

MA_DATA176

MA_DATA177

MA_DATA178

MA_DATA179

MA_DATA180

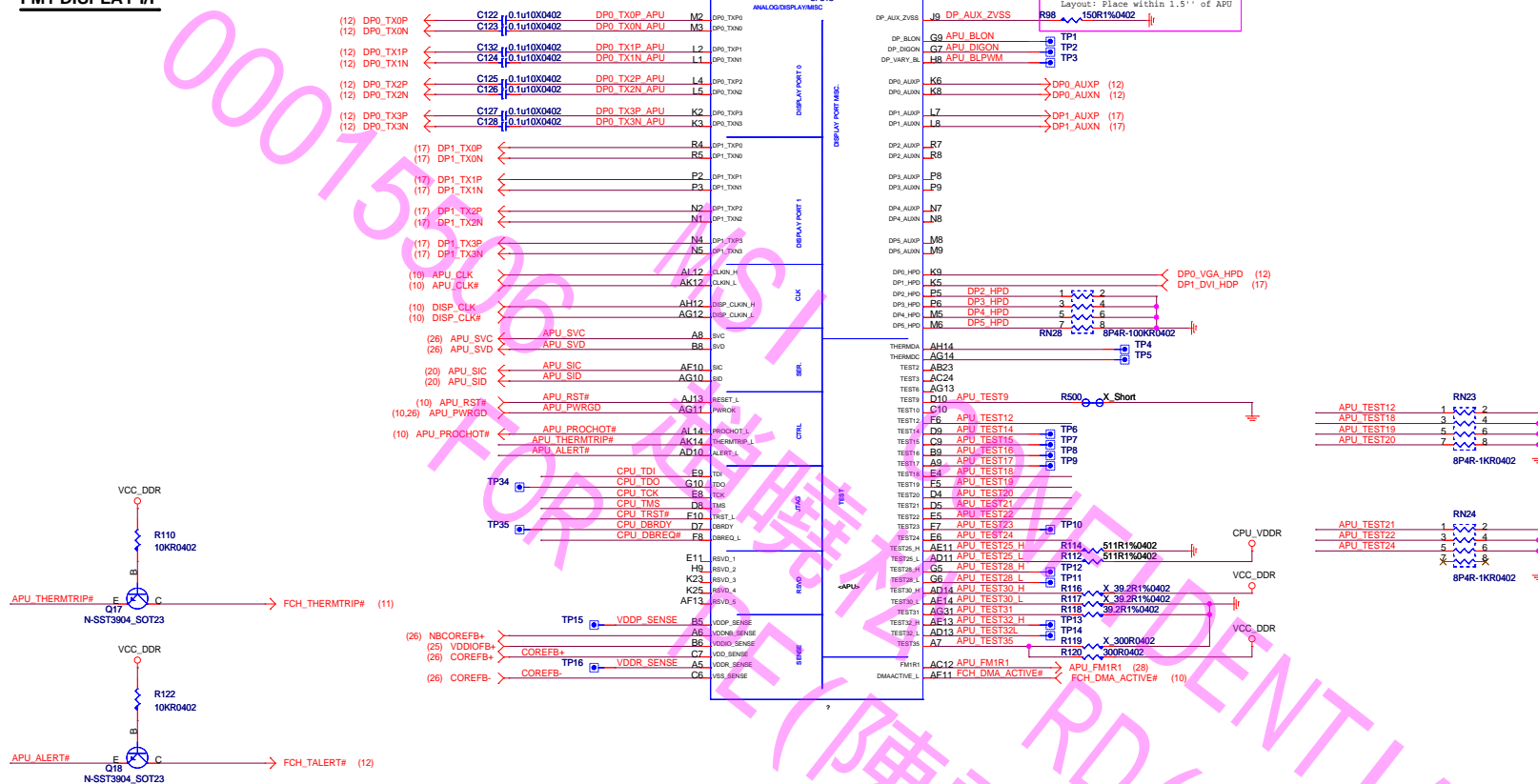
MA_DATA181

MA_DATA182

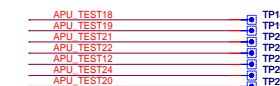
MA_DATA183

MA_DATA184

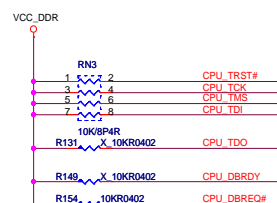
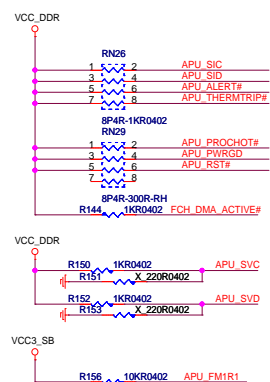
FM1 DISPLAY I/F

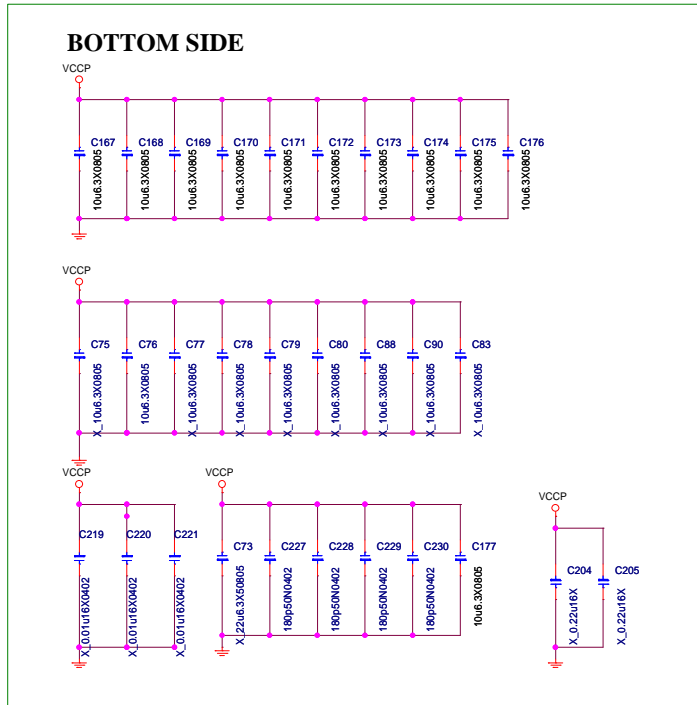
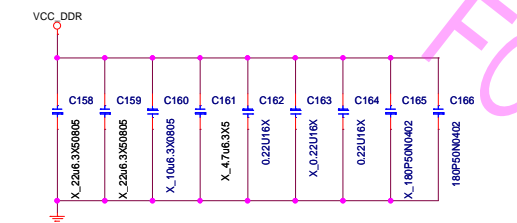
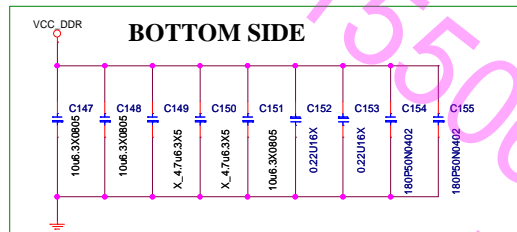
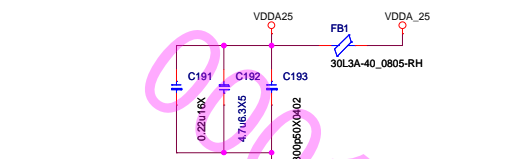


SCAN Connector

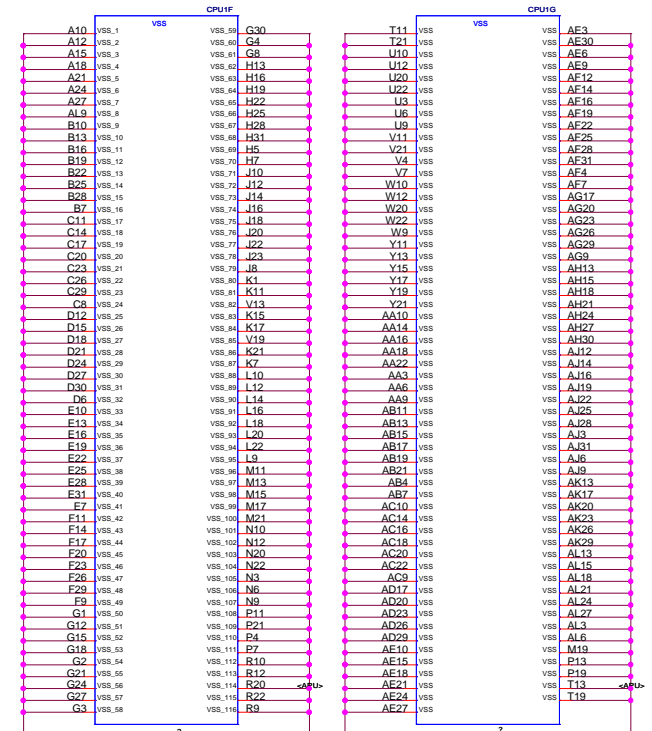
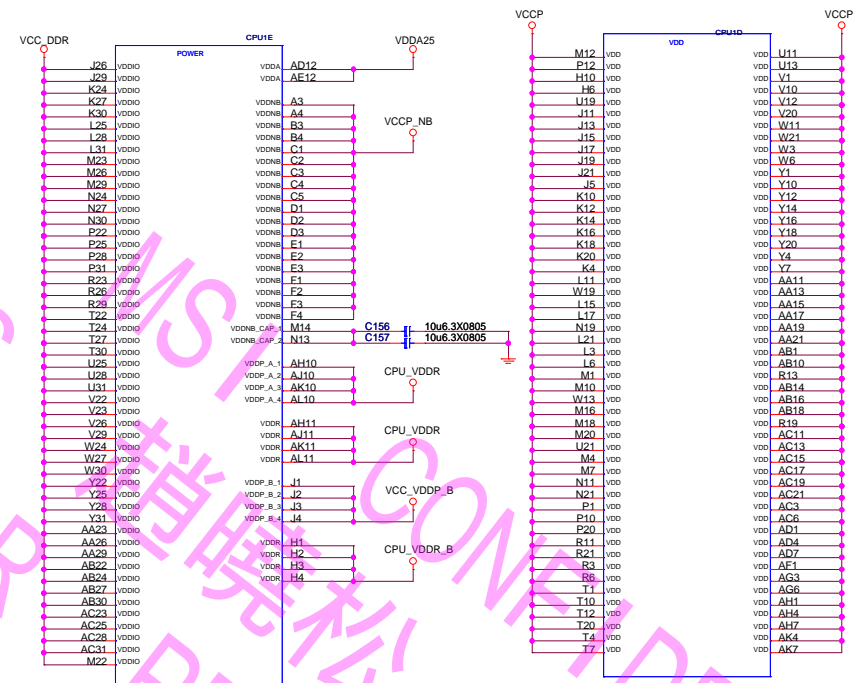
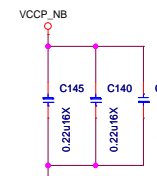
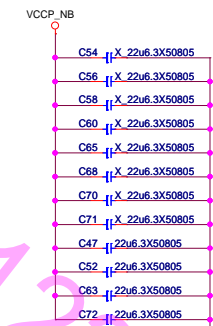
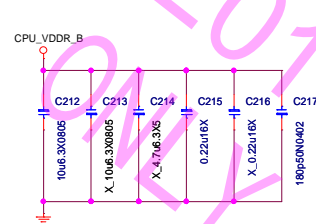
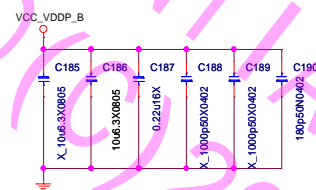
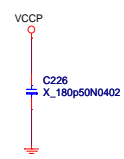
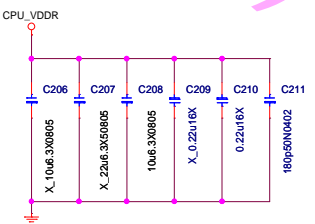
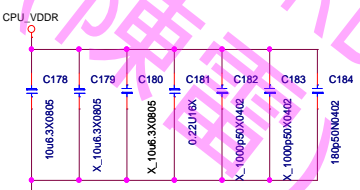


PULL UP





VDDP and VDDR support two separate power planes with single regulator



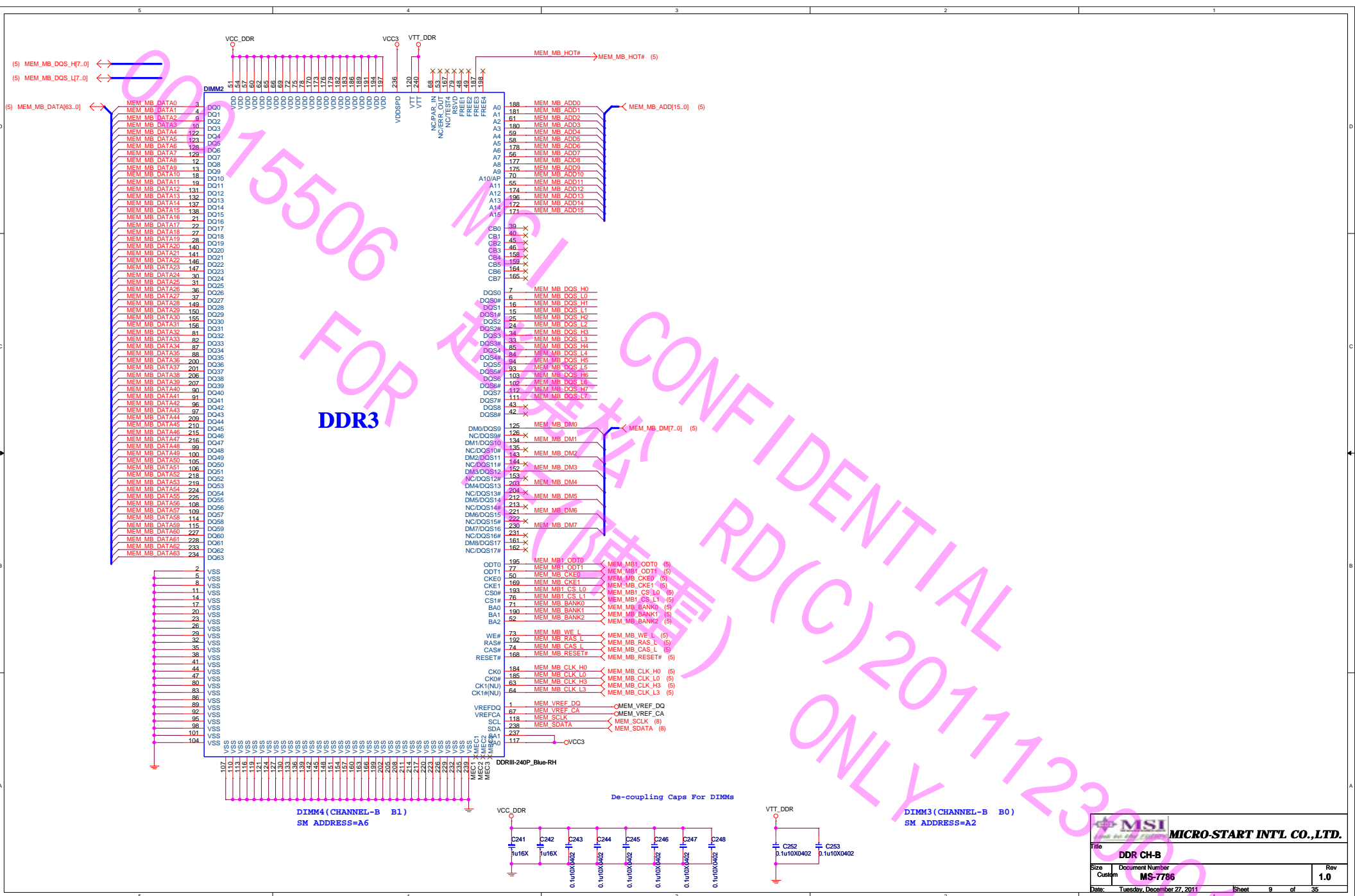
FM1 POWER&DECOUPLING		
Size	Document Number	Rev
Custom	MS-7786	1.0
Date:	Tuesday, December 27, 2011	Sheet 7 of 35

DDR3

DIMM2 (CHANNEL-A A1)
SM ADDRESS=A4

DIMM1 (CHANNEL-A A0)
SM ADDRESS=A0

MSI MICRO-START INT'L CO.,LTD.	
Title: DDR CH-A	
Size: Custom	Document Number: MS-7786
Date: Tuesday, December 27, 2011	Sheet: 8 of 35
Rev: 1.0	

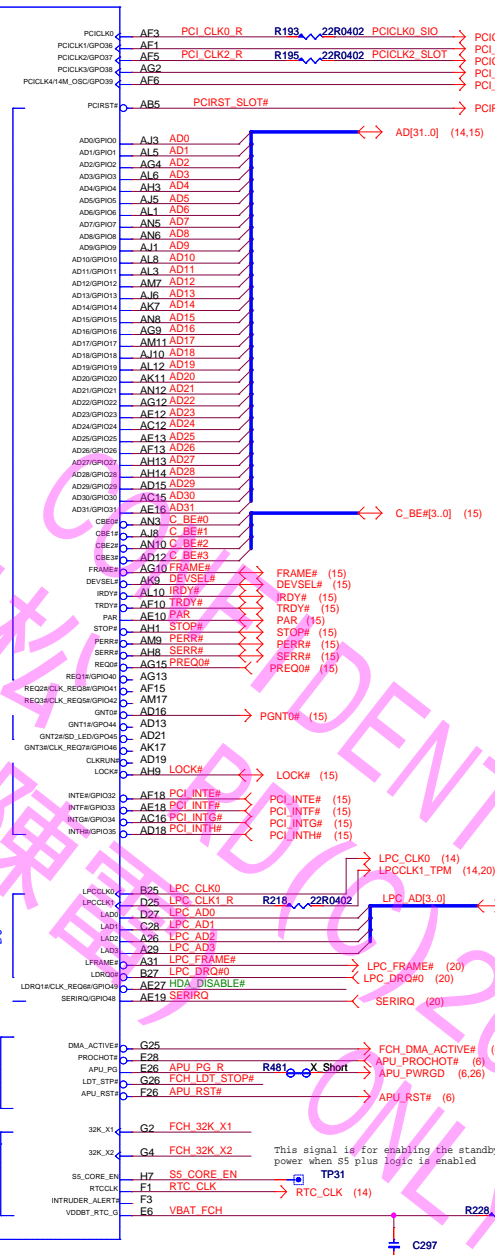
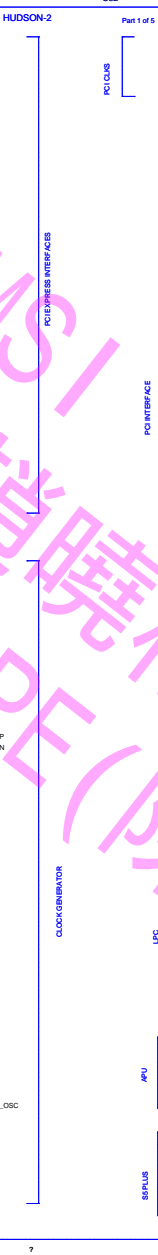
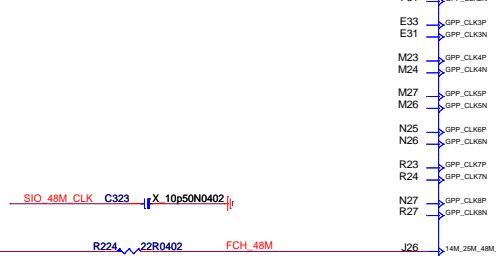
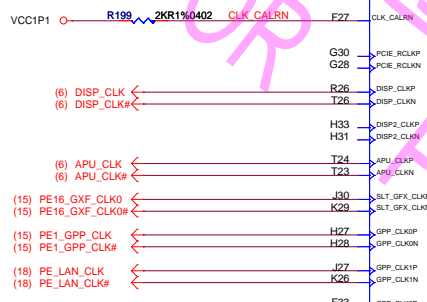
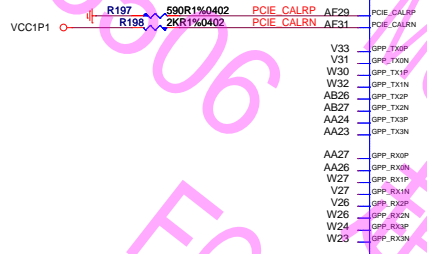
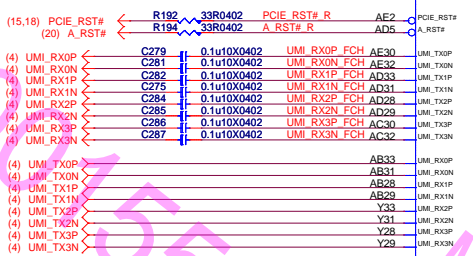


To PCIEX16, X1, LAN
To SIO

PCIE_RST#
A_RST#

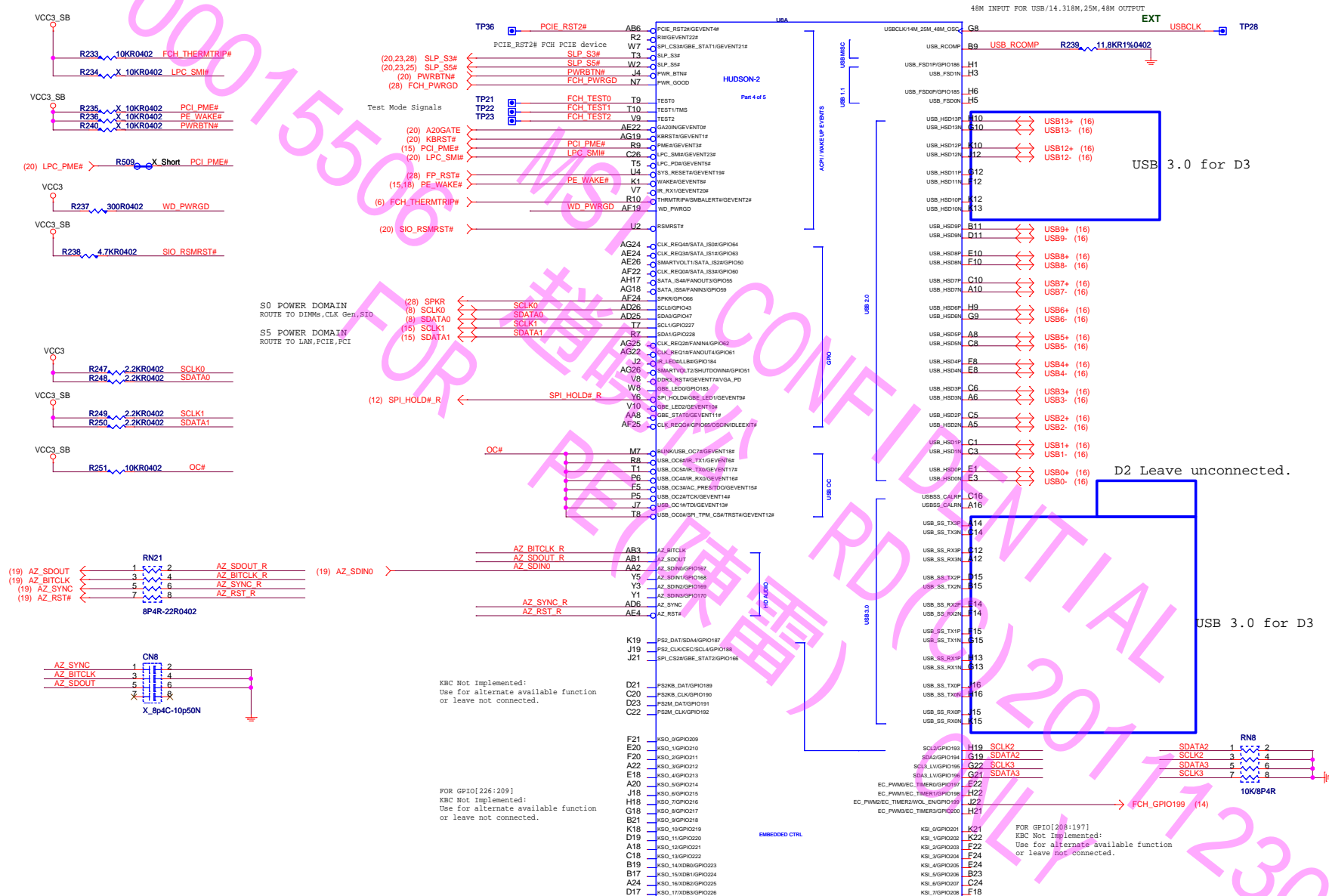
C277 150p25N0402
C280 150p25N0402

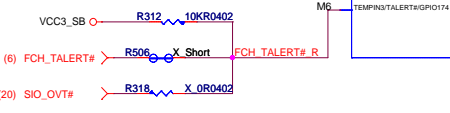
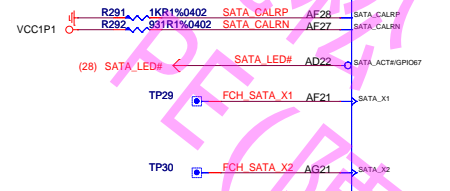
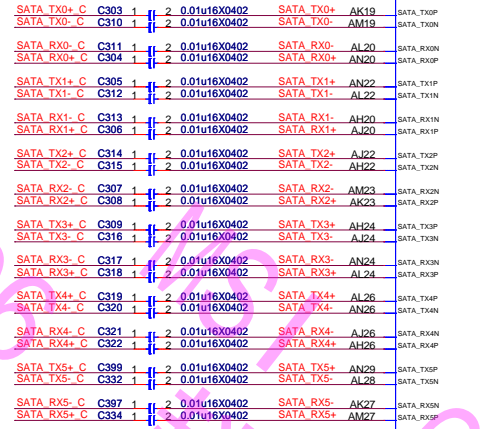
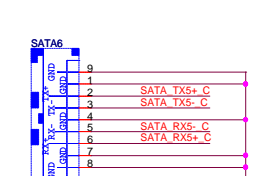
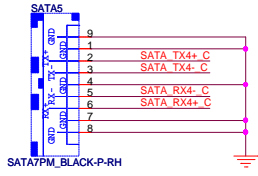
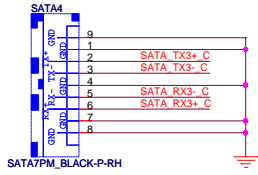
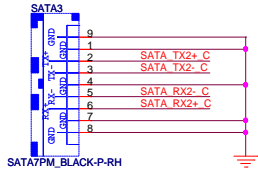
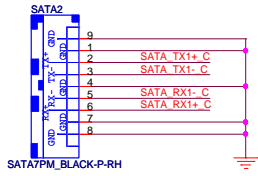
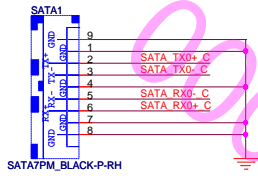
A_RST# for LPC device:
PCIE_RST# for APU PCIE device:
PCIE_RST# FCH PCIE device



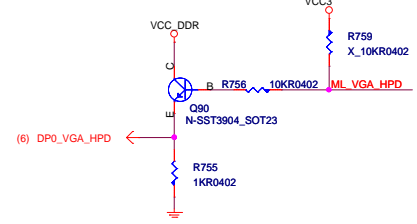
Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the APU I/O rail. They are also in the S5 domain to prevent glitching at power up.

HUDSON ACPI/USB/AZ/GPIO

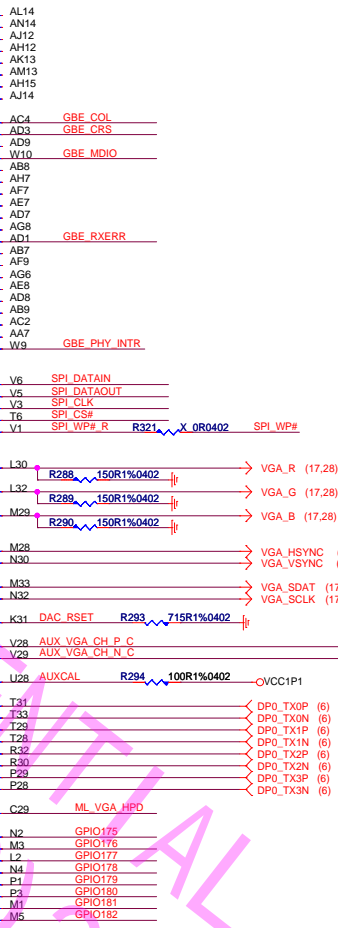
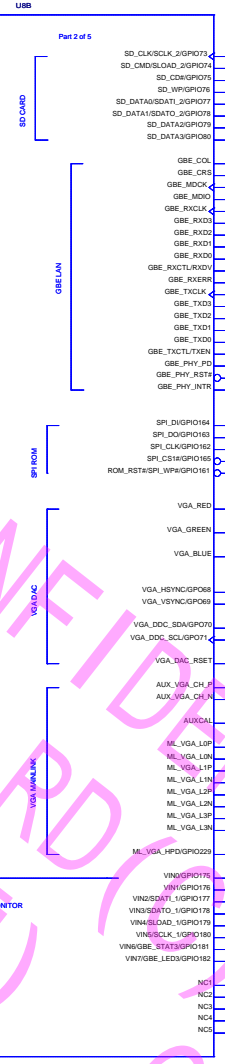
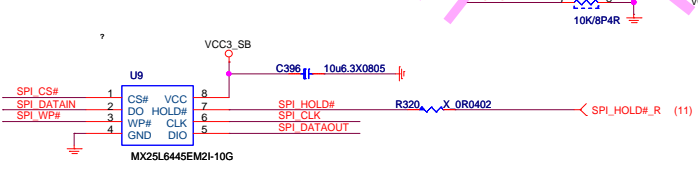




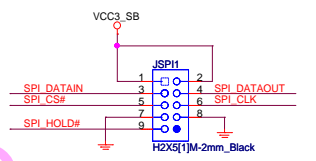
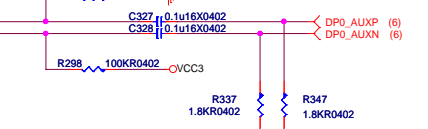
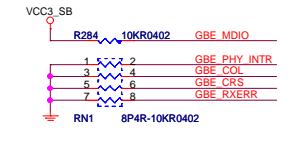
VGA HPD



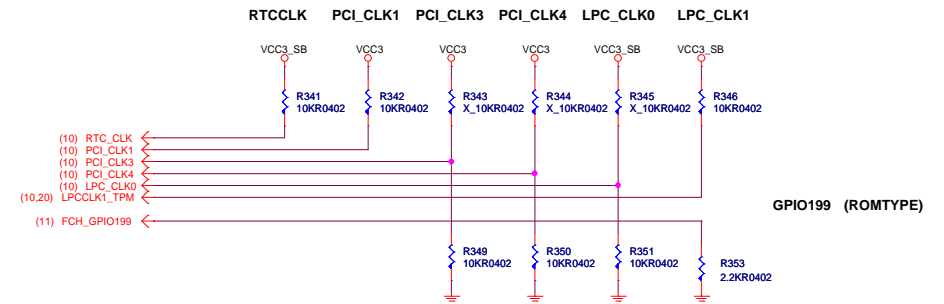
SPI ROM & DEBUG HEADER



GBE NOT ENABLED



FCH REQUIRED STRAPS



	RTCCCLK	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO199 (ROMTYPE)
PULL HIGH	S5 Plus MODE DISABLED DEFAULT	PCIe interface at Gen2 DEFAULT	Enable Debug Straps	Reserved	EC ENABLED	Internal clock mode DEFAULT	LPC ROM
PULL LOW	S5 Plus MODE ENABLED	FORCE PCIe at Gen1	Disable Debug Straps DEFAULT	APU_CLK/DISP_CLK Required setting DEFAULT	EC DISABLED DEFAULT	External clock mode	SPI ROM DEFAULT

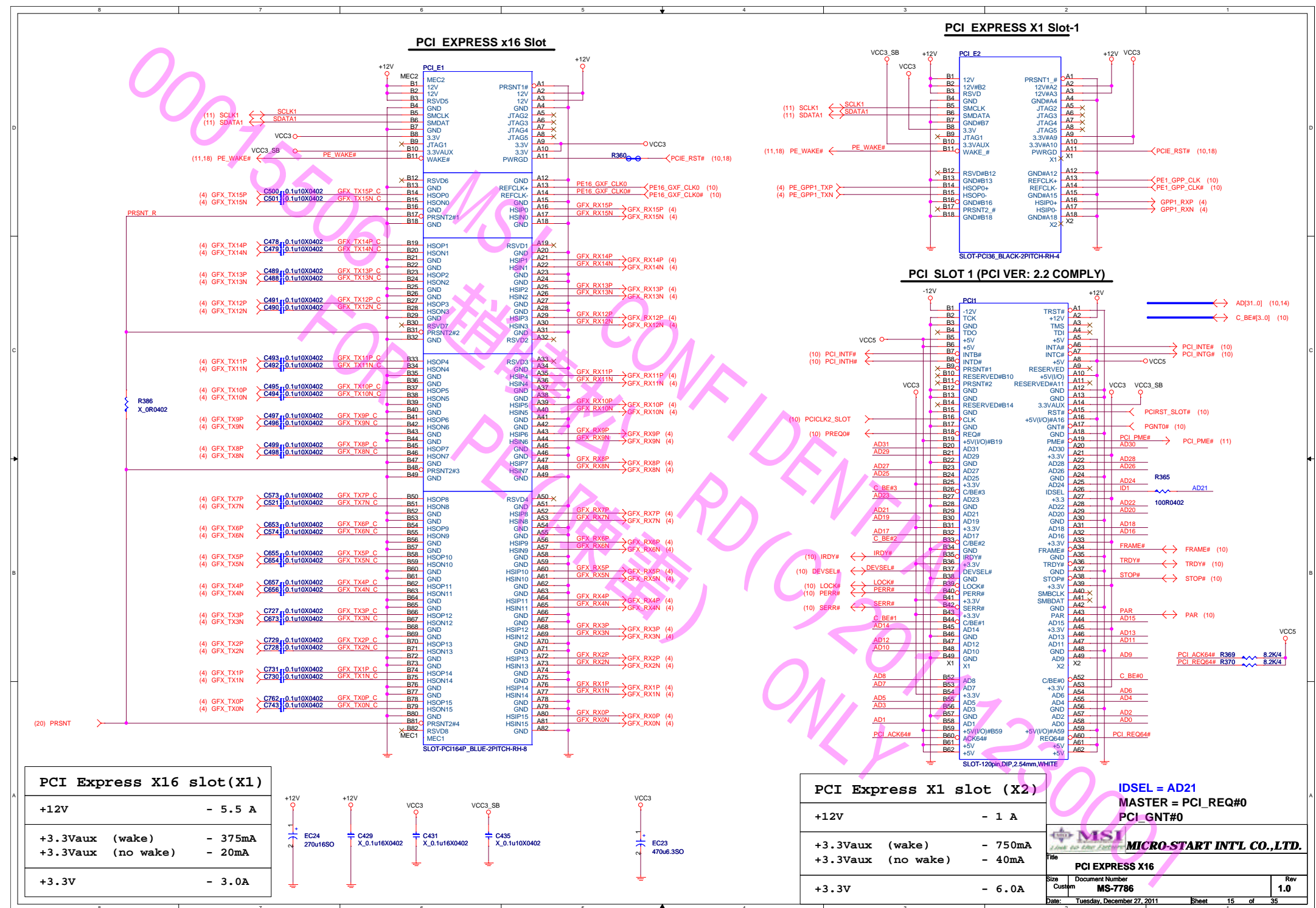
*This strap is not used in External clock mode

FCH DEBUG STRAPS

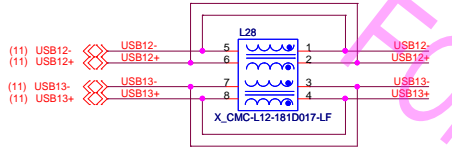
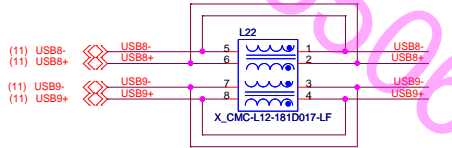
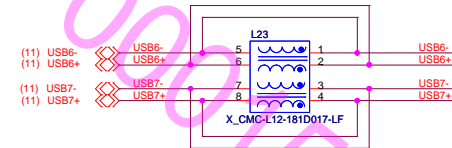


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	Use internal PLL clock DEFAULT			Disable I2C ROM DEFAULT	Use ROMTYPE straps DEFAULT
PULL DOWN	Bypass Internal PLL clock			Enable loading settings for UMI/PLL/misc from I2C ROM	Boot from PCI bus

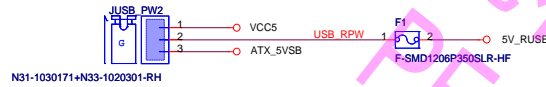
Layout:
VSSPL_SYS/VSSAN_HMM CONNECT TO GND
WITH A SEPERATED VIA



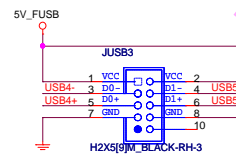
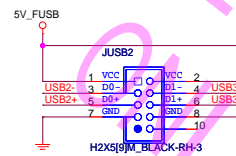
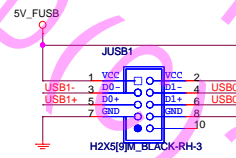
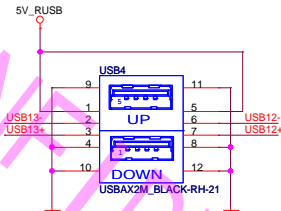
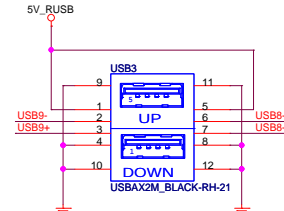
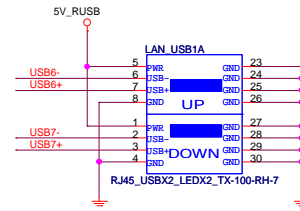
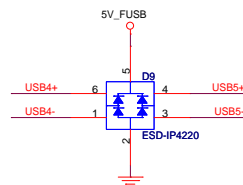
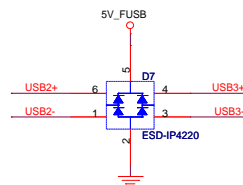
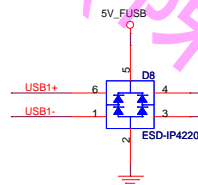
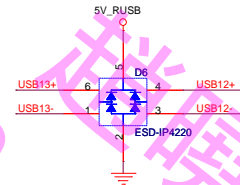
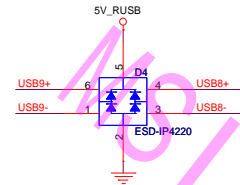
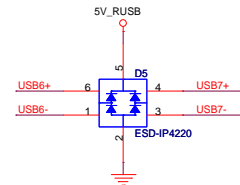
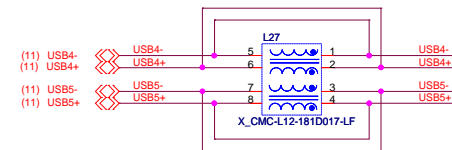
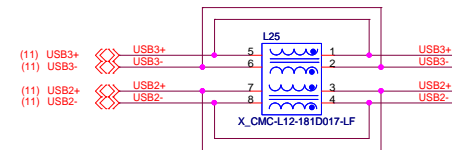
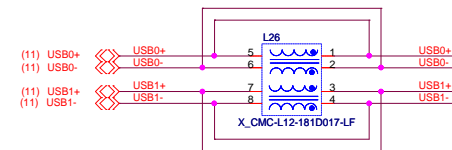
POWER CIRCUIT FOR USB PORT 0,1



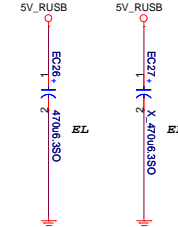
Near Rear ==>



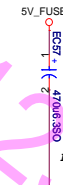
Near Front ==>



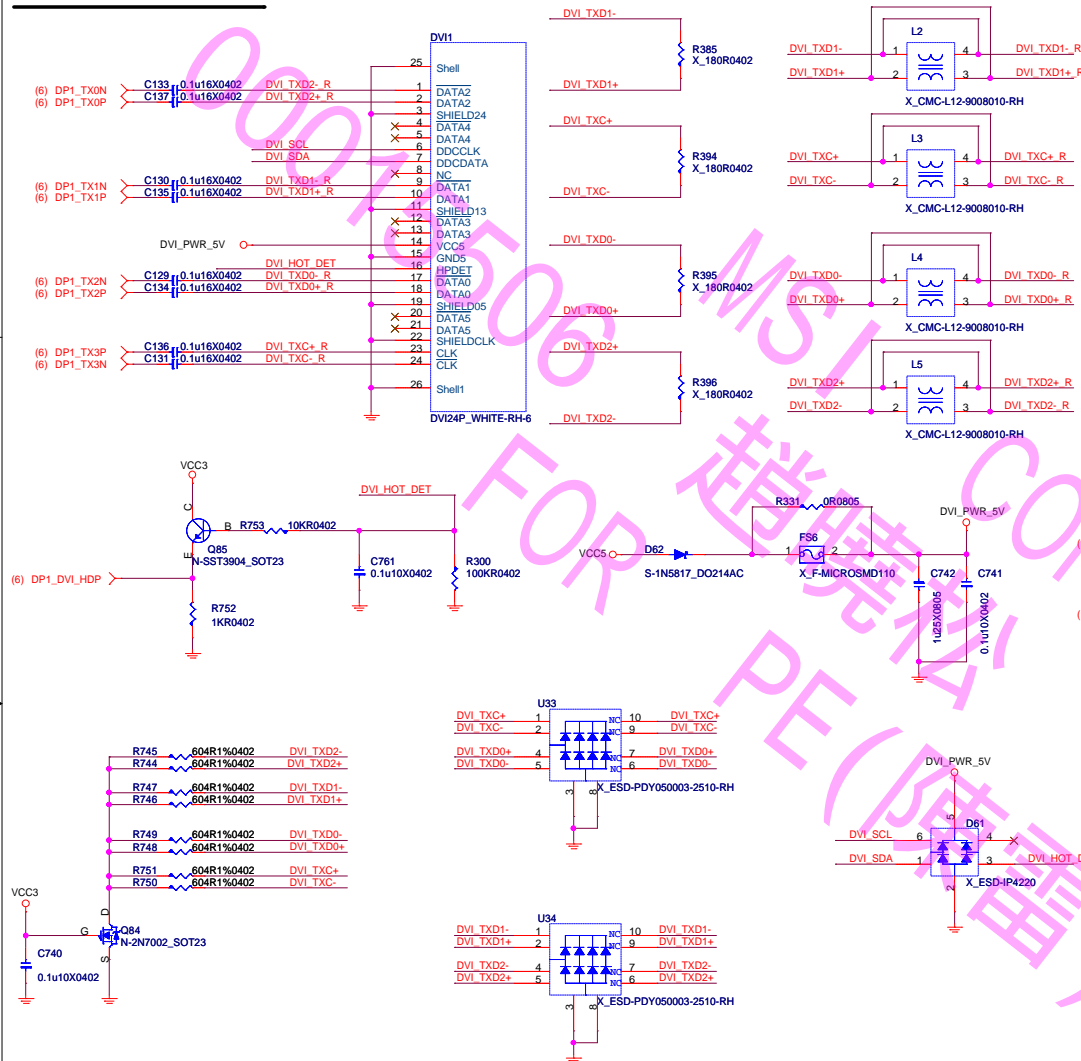
NEAR USB REAR CONNECTOR



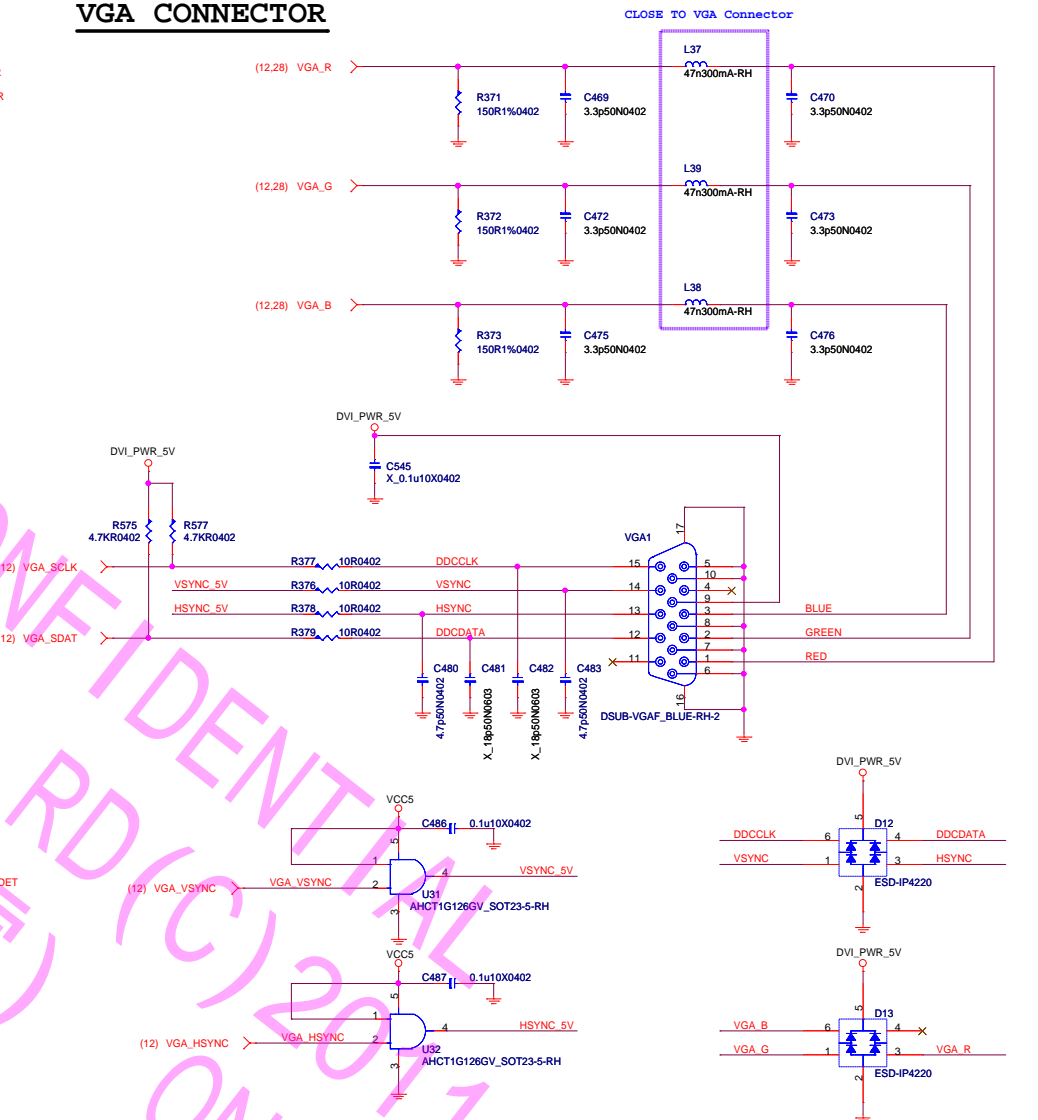
NEAR USB Front CONNECTOR



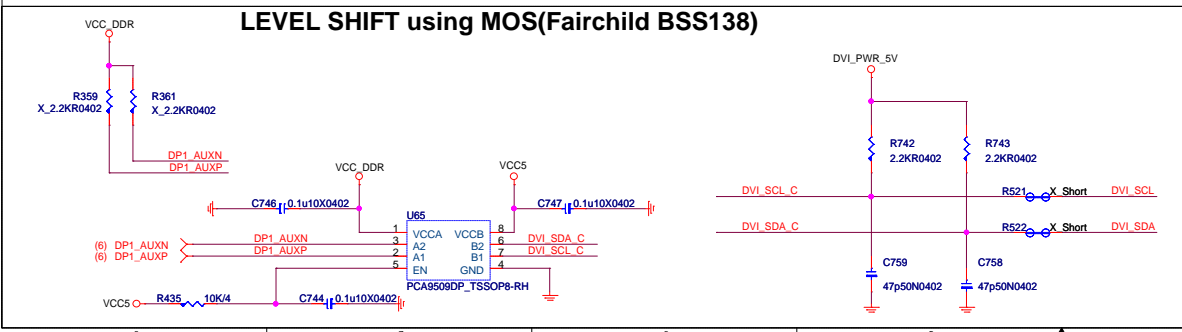
DVI CONNECTOR



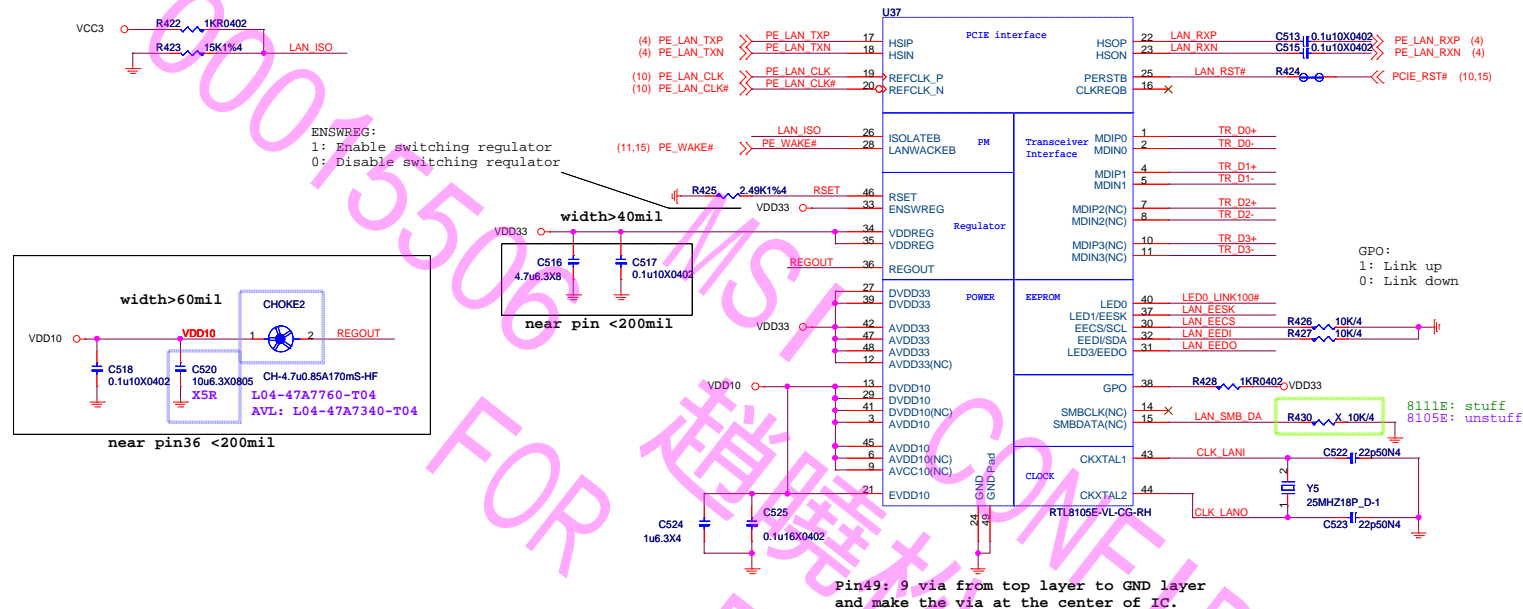
VGA CONNECTOR



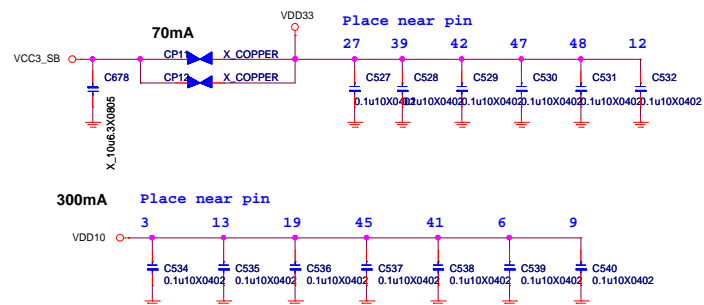
LEVEL SHIFT using MOS(Fairchild BSS138)



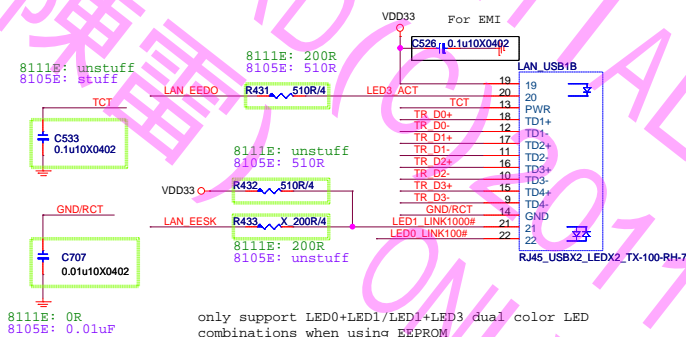
RTL8105E/Co-Lay 8111E



3.3v Power on rise time : 1~100ms.











LAN Connector



only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM

2pF	1pF
D0G-0200529-A68	D0G-0422003-P03
D0G-0303309-C12	D0G-0422003-N47

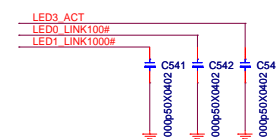
Giga-Lan		10/100-Lan	
N58-22F0731		N58-22F0771	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19		19	
20	 Yellow	20	 Yellow
	Orange		
21		21	
22	 Green	22	 Green

8105E POWER Consumption

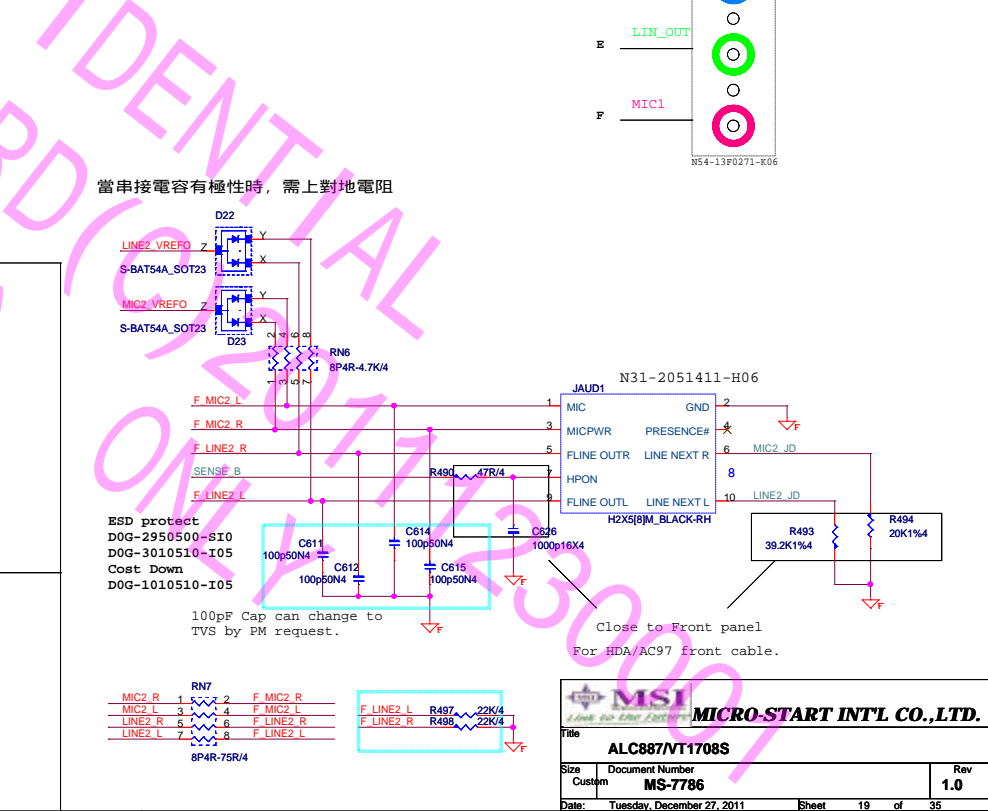
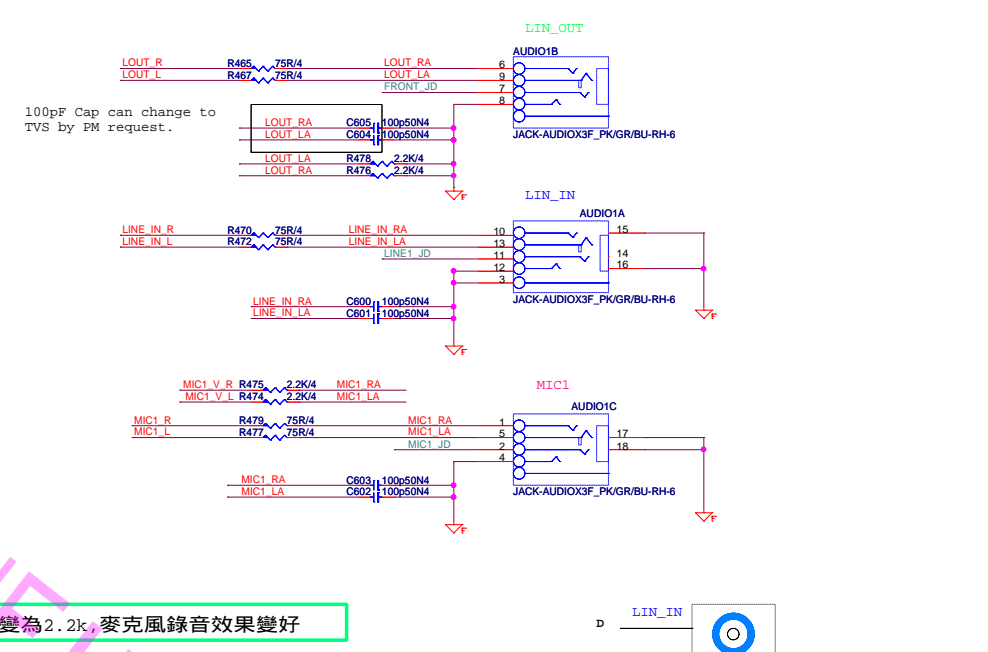
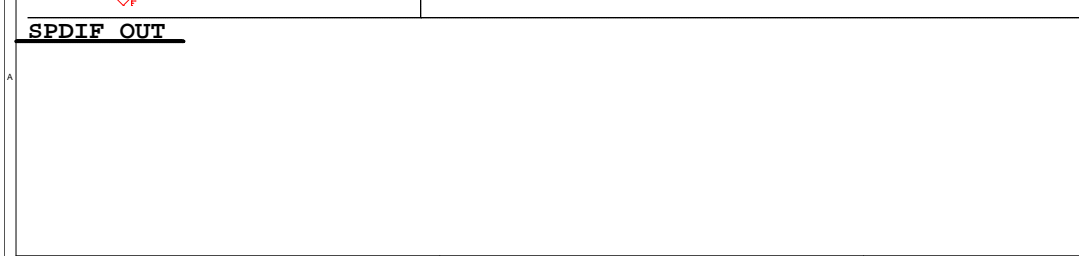
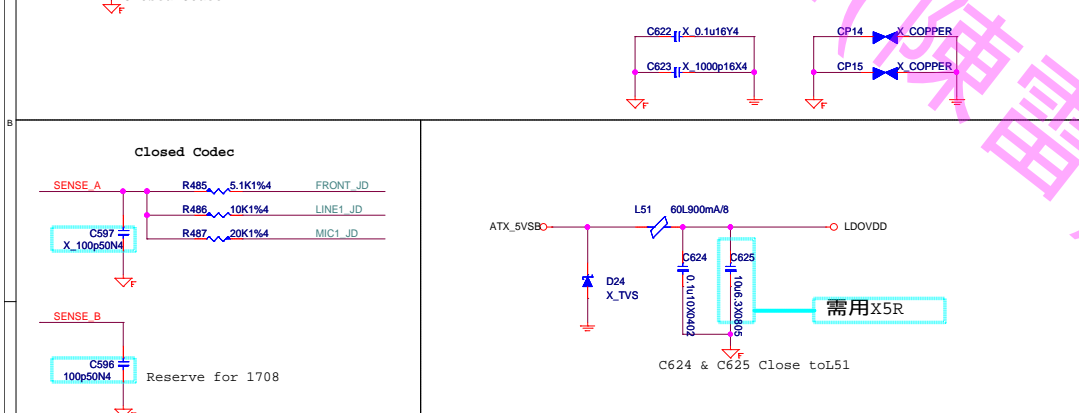
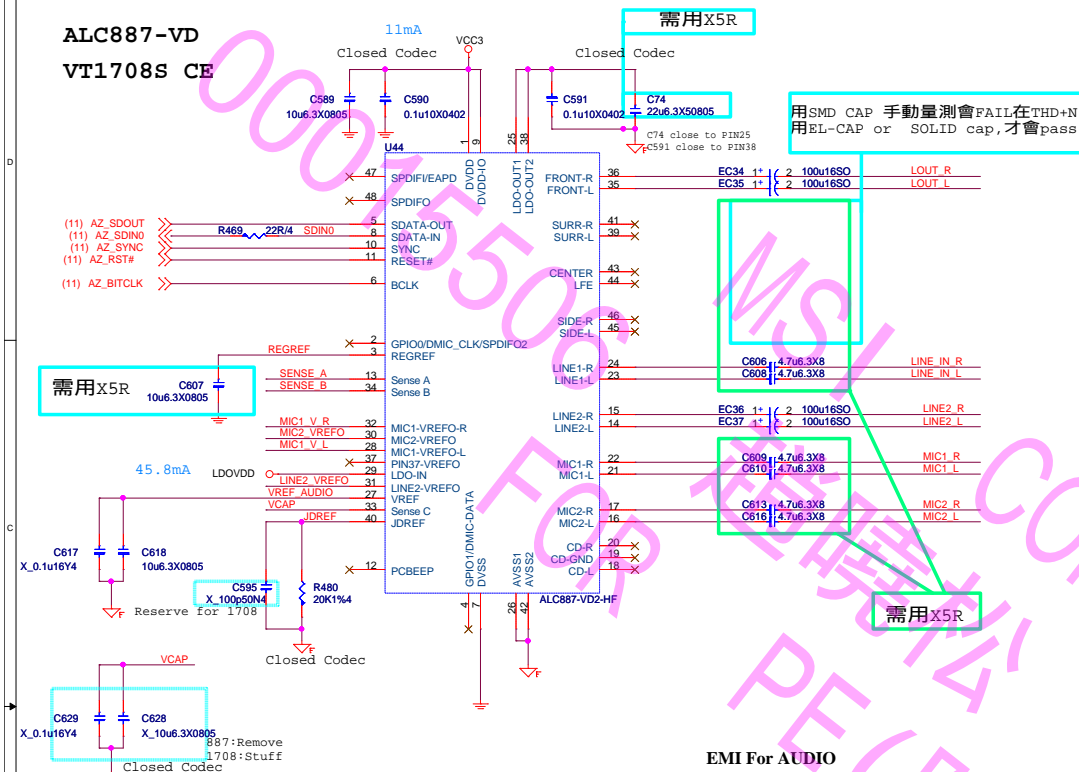
	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

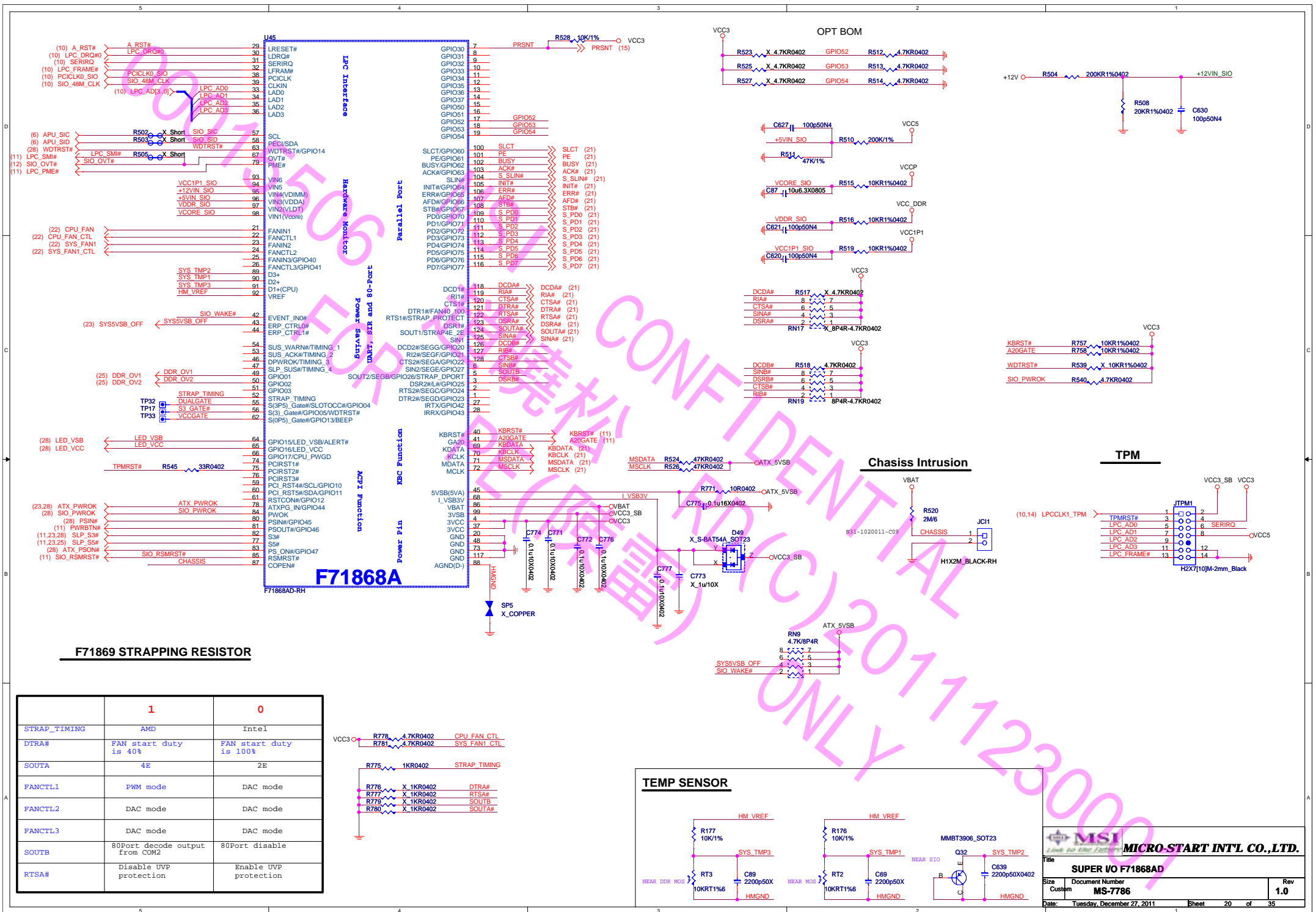
8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

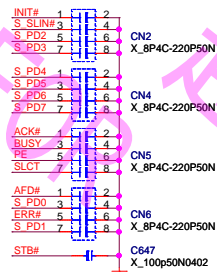
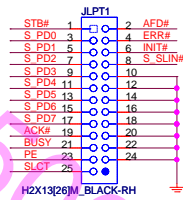
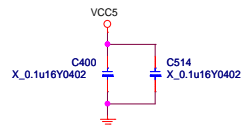
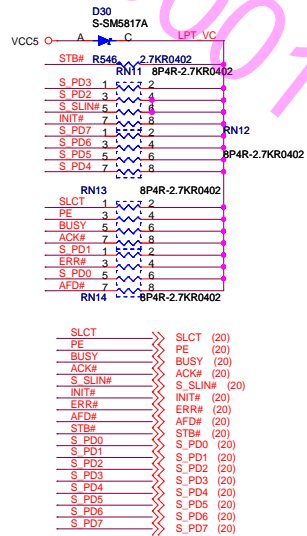


ALC887-VD
VT1708S CE

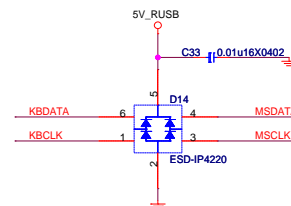
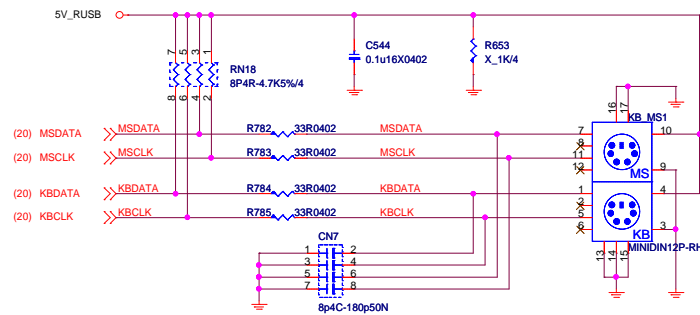
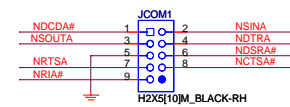
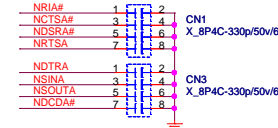
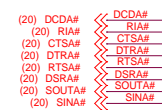
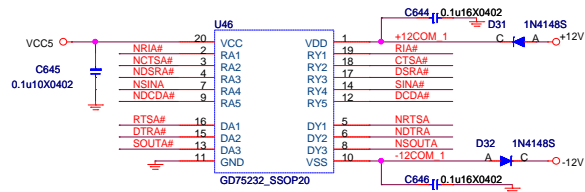




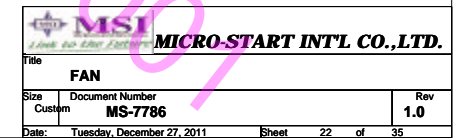
PARALLAL PORT



SERIAL PORT 1

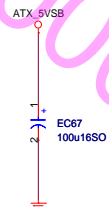


(Default)

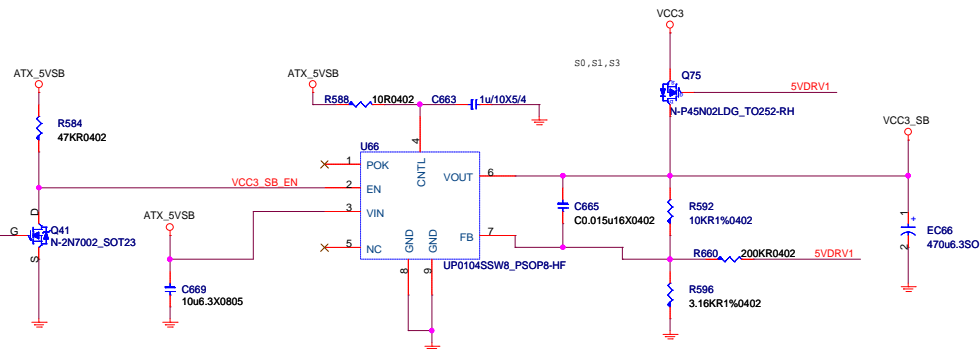


VCC5_SB Power Switch

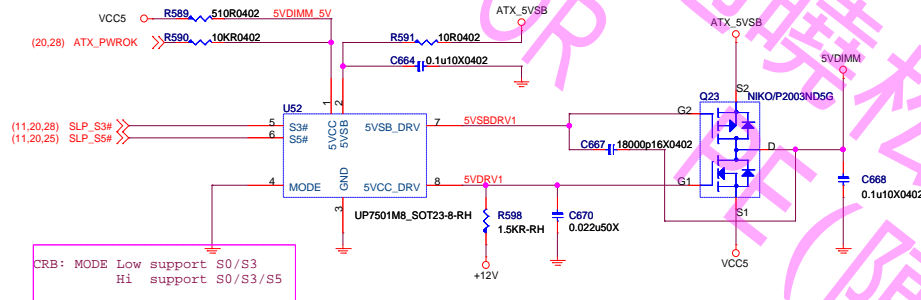
Trace Width 80mils.



VCC3_SB POWER



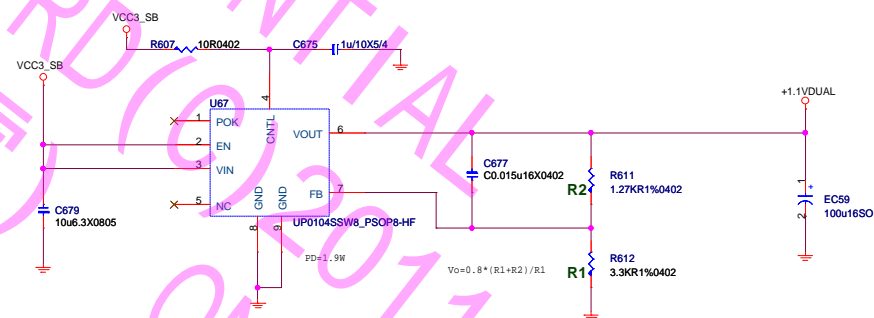
5VDIMM FOR DDR



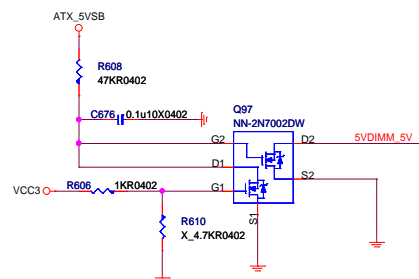
1.1VDUAL POWER

$$(3.3-1.1) \times 1.3 = 2.86W > P_o$$

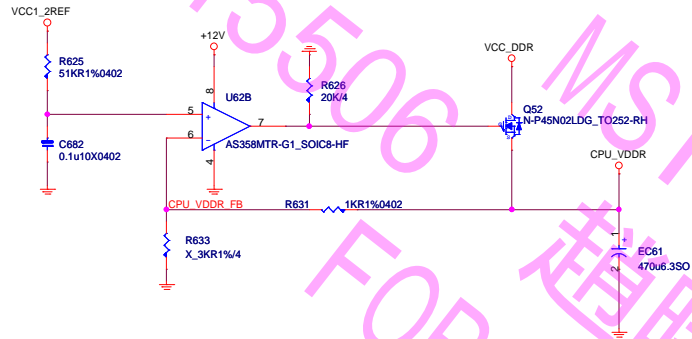
1.1V@1.3A



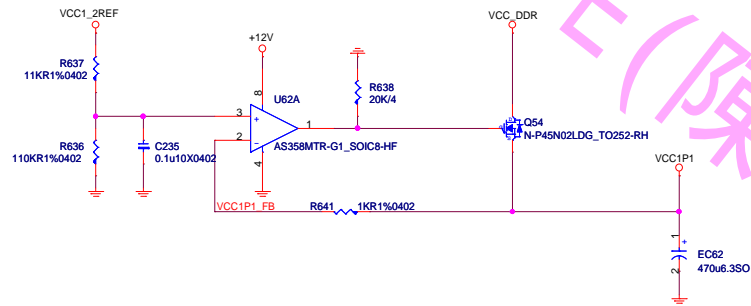
For special PSU sequence



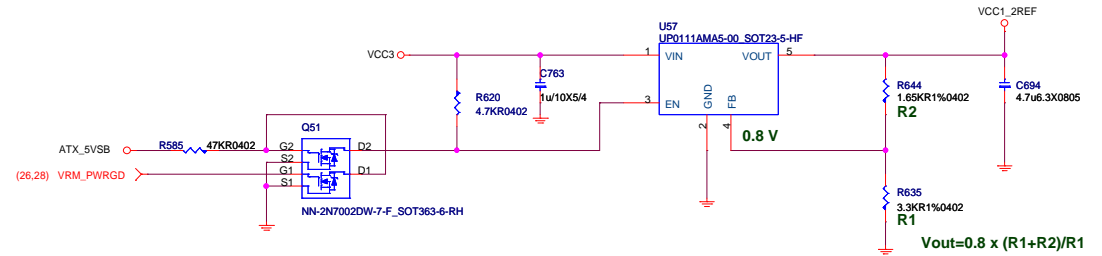
CPU_VDDP + CPU_VDDR POWER 1.2 V@3.2A



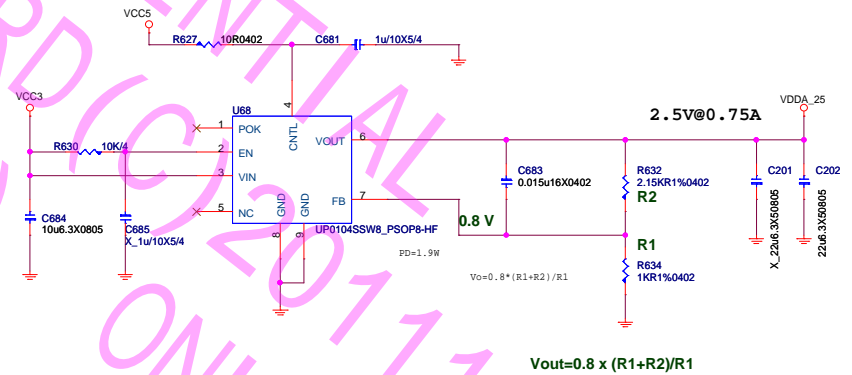
VCC1P1 POWER 1.1V@2A



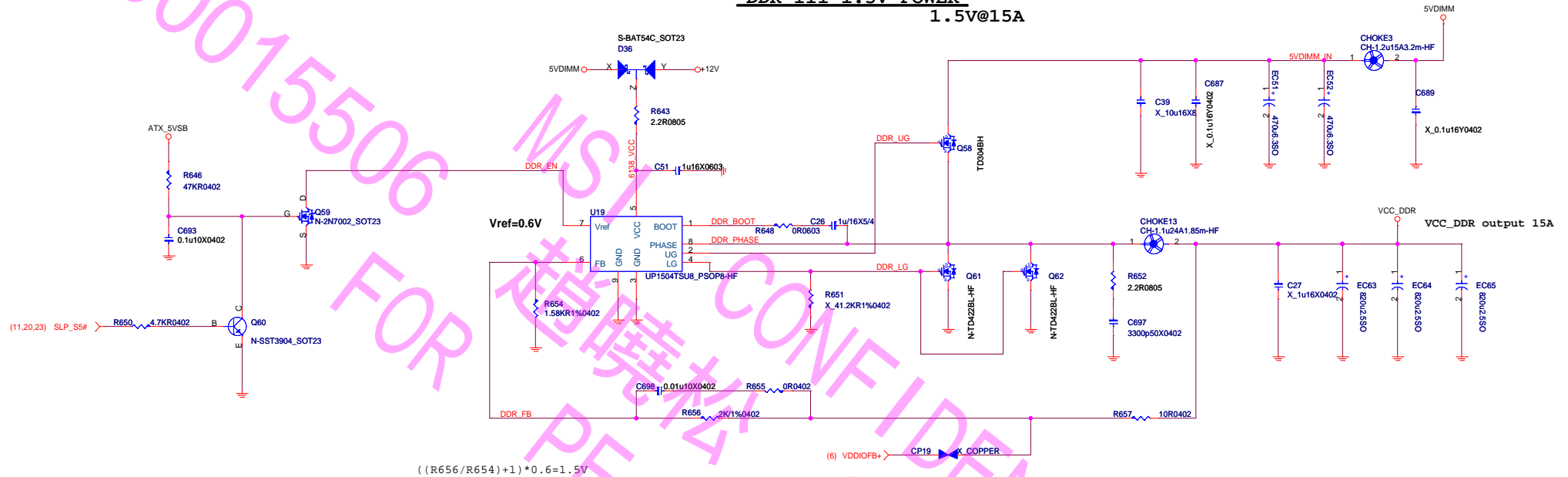
VCC1_2REF



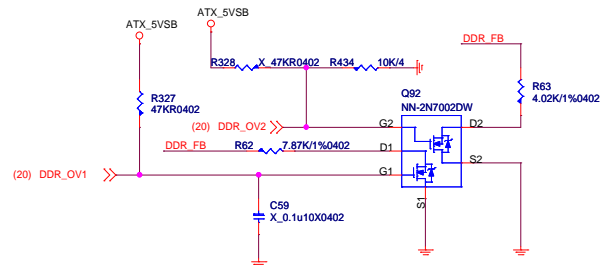
CPU VDDA_25 POWER



DDR III 1.5V POWER
1.5V@15A

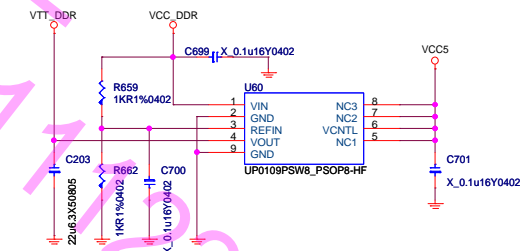


OV

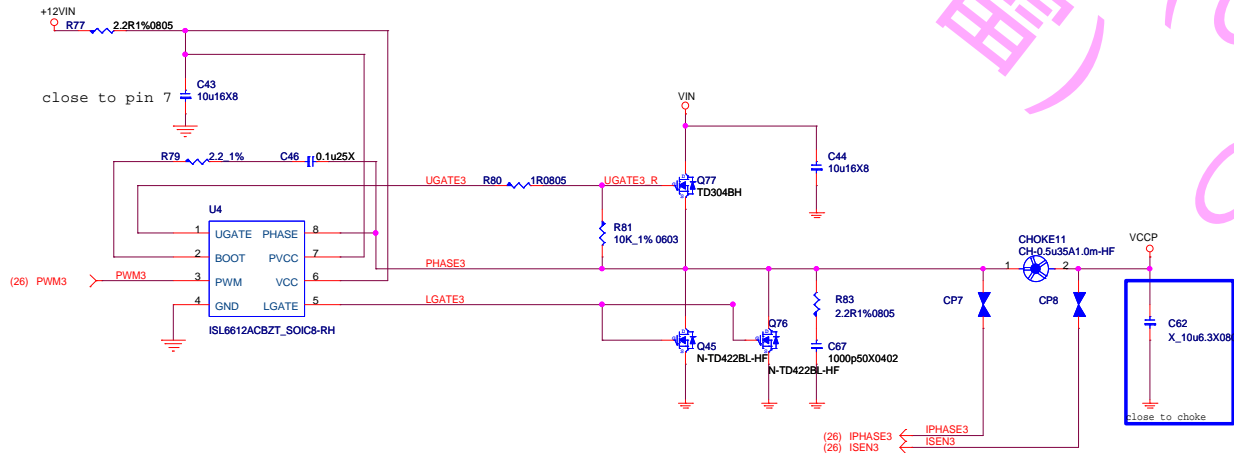
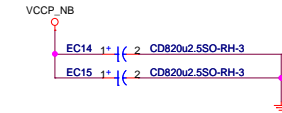
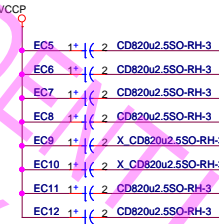
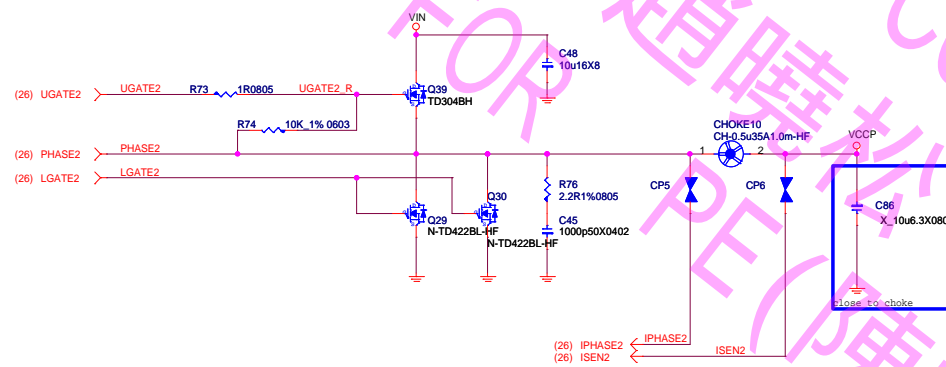
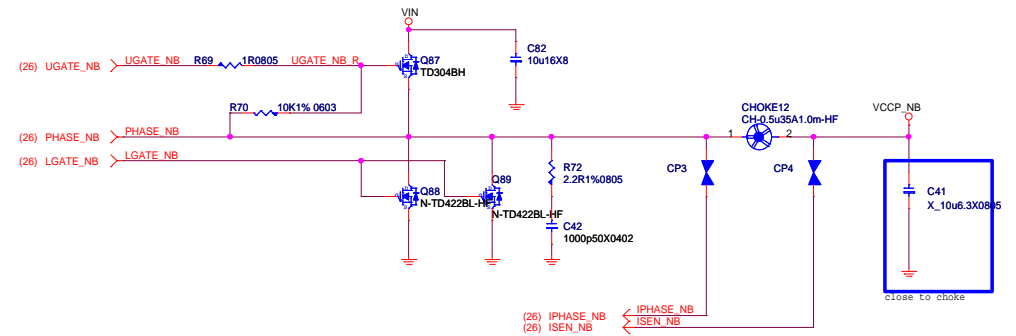
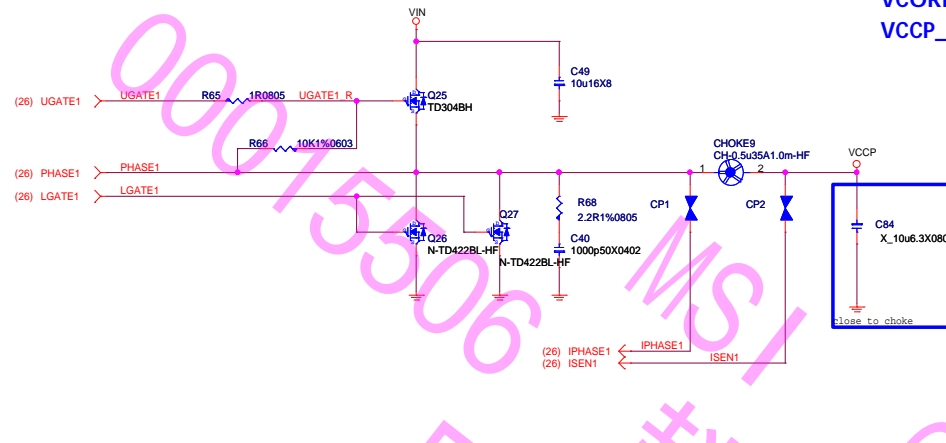


MODE	第一階	Default	第二階	第三階
DDR_OV1	LOW	HIGH	LOW	HIGH
DDR_OV2	LOW	LOW	HIGH	HIGH
VALUE	1.35V	1.5V	1.65V	1.8V

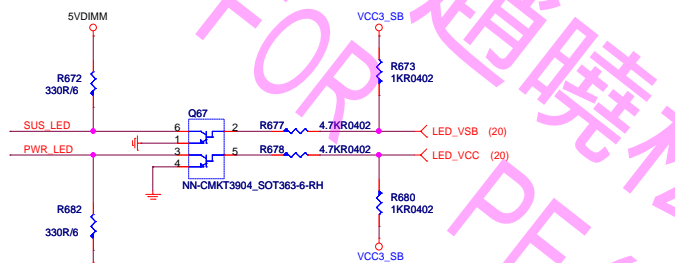
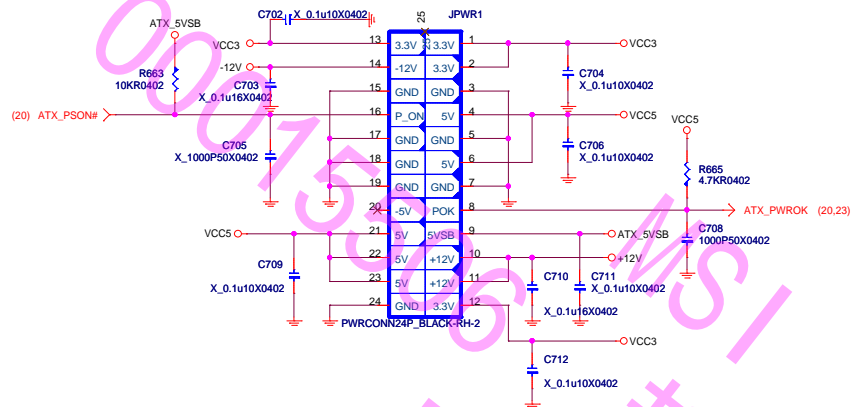
0.75V@2A VTT_DDR POWER



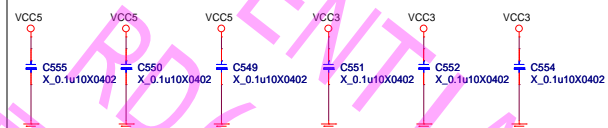
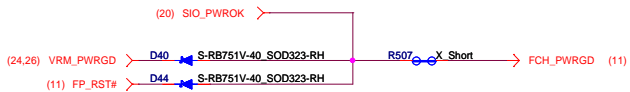
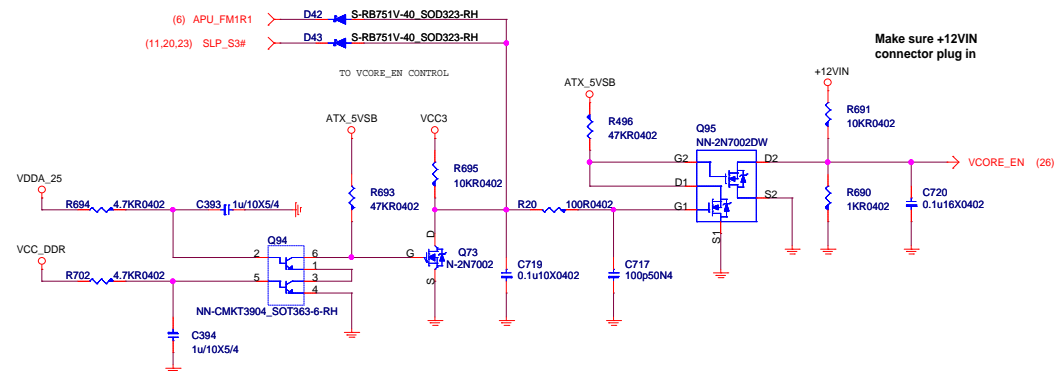
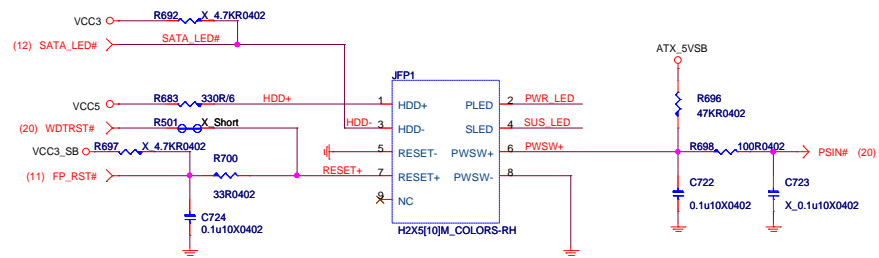
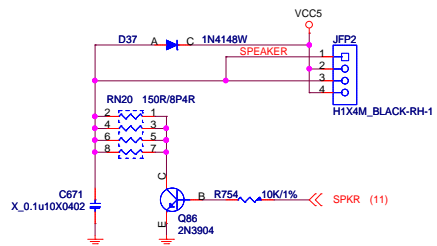
VCORE 100A TDC:80A
VCCP_NB 32.5A TDC:26A



ATX CONNECTOR



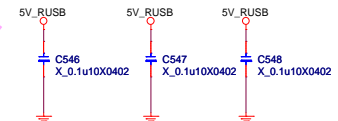
BUZZER



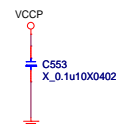
EMI For VGA



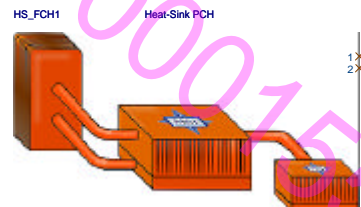
EMI For REAR USB



EMI For VCCP



HEAT SINK



LA1



AMD-218-0755064-A13-RH



RTL8111E-VL-CG-RH



CD470u16EL11.5

R



OR0402



SATA7PM_BLACK-P-RH



RTL8111E-Connector



CD1000u63EL11.5-RH



USBAX2M_BLACK-RH-20



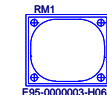
CD100u25EL11-RH

MANUAL PART



BAT1_X1
BAT-CR2032-RH

AVL:
D06-0100161-P52
D06-0100101-K26



E95-0000003-H06



E93-0000094-C22

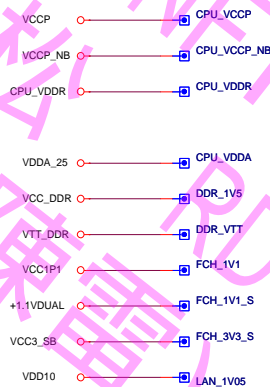


681-7786-A10
LABEL

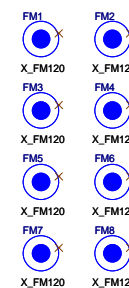


7786-1.0

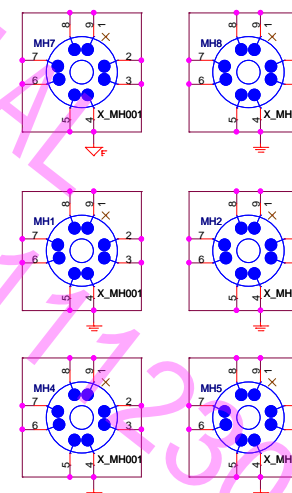
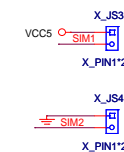
PK0-0778610-037, 精成, 23, 寶安恩斯邁廠 (MSIS)
PK0-0778610-037, 精成, 7, 寶安恩斯邁廠 (MSIS)
PK0-0778610-048, 競華, 23, 寶安恩斯邁廠 (MSIS)
PK0-0778610-048, 競華, 7, 寶安恩斯邁廠 (MSIS)



Optics Orientation Holes



Simulation



MSI MICRO-START INT'L CO.,LTD.	
File Auto BOM Manual	
Size Custom	Document Number MS-7786
Date Tuesday, December 27, 2011	Sheet 29 of 35
Rev 1.0	

0A
Circuits

2011.11.01 Modify from 7697-1.0
Remove PCI-Ex1 & USB3.0 & One DDR High side MOS
Combine with CPU_VDDP & CPU_VDDR Power

2011.11.21 Guber out

1.0
Circuits

2011.12.22 Guber out

BOM

2011.12.23 Modify DVI & PWM MON

2011.06.28

2011.07.26

2011.07.27

2011.08.03


2011.08.04

2011.08.05

2011.08.12

2011.08.16

2011.08.22

		MICRO-START INTL CO.,LTD.	
History			
File			
Size	Document Number	Rev	
Custom	MS-7786	1.0	
Date:	Tuesday, December 27, 2011	Sheet	30 of 35